Listing and Amendments to the Claims

This listing of claims will replace the claims that were published in the PCT Application:

1. (currently amended) An address generation apparatus for one of an interleaver and a deinterleaver in a Wideband Code Division Multiple Access (W-CDMA) system, the apparatus comprising:

at least one memory device; and

an address pair generator ~~(300)~~ for generating an address pair (n, P(n)) in real-time for one of an interleaver operation and a deinterleaver operation that includes inter-row permutation and intra-row permutation,

wherein the address pair (n, P(n)) is generated such that, for the interleaving operation, data to be interleaved are read out from the at least one memory device using the P(n) and interleaved data are written into the at least one memory device using the n, and

wherein the address pair (n, P(n)) is generated such that, for the deinterleaving operation, data to be deinterleaved are read out from the at least one memory device using the n and deinterleaved data are written into the at least one memory device using the P(n).

2. (currently amended) The address generation apparatus of claim 1, further comprising at least one memory device ~~(350)~~, and wherein patterns for the inter-row permutation and the intra-row permutation are stored in said at least one memory device prior to the one of the interleaver operation and the deinterleaver operation.

3. (original) The address generation apparatus of claim 1, wherein the interleaver and the deinterleaver are of a block type.

4. (original) The address generation apparatus of claim 1, wherein the interleaver and the deinterleaver are of a Turbo type.

5. (currently amended) A method of address generation for at least one of an interleaver and a deinterleaver in a Wideband Code Division Multiple Access (W-CDMA) system, the method comprising the steps of:

generating ~~(250)~~ an address pair (n, P(n)) in real-time for one of an interleaver operation and a deinterleaver operation that includes inter-row permutation and intra-row permutation,

wherein the address pair (n, P(n)) is generated such that, for the interleaving operation, data to be interleaved are read out from the at least one memory device using the P(n) and interleaved data are written into the at least one memory device using the n, and

wherein the address pair (n, P(n)) is generated such that, for the deinterleaving operation, data to be deinterleaved are read out from the at least one memory device

using the n and deinterleaved data are written into the at least one memory device using the P(n).

6. (currently amended) The method of claim 5, further comprising the step of pre-storing ~~(350)~~ patterns for the inter-row permutation and the intra-row permutation prior to the one of the interleaving operation and the deinterleaving operation.

7. (original) The method of claim 5, wherein the interleaver and the deinterleaver are of a block type.

8. (original) The method of claim 5, wherein the interleaver and the deinterleaver are of a Turbo type.

9. (currently amended) A method of real-time address generation for an interleaver in a Wideband Code Division Multiple Access (W-CDMA) system, the interleaver for interleaving a data sequence having a length K, the method comprising the steps of:

computing ~~(220)~~ a row value X_r and a column value X_c using a number of rows in an interleaver matrix;

computing ~~(230)~~ a new row value $X_{r,new}$ and a new column value $X_{c,new}$ according to a row permutation function $PR(X_r)$ and column permutation function $PC(T(X_r,X_c))$; and

generating ~~(250)~~ an address pair (n, P(n)) for an interleaver operation when the P(n) is less than a length of the data sequence K, the address pair (n, P(n)) being

generated such that data to be interleaved are read out from at least one memory device using the P(n) and interleaved data are written into the at least one memory device using the n, and

wherein $P(n) = (X_{r,new} * C + X_{c,new})$, and the C is a number of columns in the matrix.

10. (currently amended) The method of claim 9, further comprising the steps of:

initially setting ~~(210)~~ the n and a variable x to zero, prior to said step of computing the row value X_r and the column value X_c;

returning ~~(280)~~ to said step of computing the row value X_r and the column value X_c, when a current value of x is not less than a product of the number of columns in the matrix and a number of rows in the matrix.

11. (currently amended) The method of claim 9, further comprising the step of pre-storing ~~(350)~~ patterns for the inter-row permutation and the intra-row permutation prior to the interleaving operation.

12. (original) The method of claim 9, wherein the interleaver is of a block type.

13. (original) The method of claim 9, wherein the interleaver is of a Turbo type.